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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/807,153	03/24/2004	Sung-Fei Wang	WANG3231/EM	6463

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EXAMINER	
SANDVIK, BENJAMIN P	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 04/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/807,153	WANG, SUNG-FEI	
	Examiner	Art Unit	
	Ben P. Sandvik	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-21 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-21 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 3, 4, 13, 18, 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Misumi (U.S. Patent #6481870).

With respect to **claim 1**, Misumi teaches a multi-chips module package comprising

a main substrate having an upper surface and a plurality of contacts (Fig. 2, 4),

a first chip disposed above the main substrate (Fig. 2, 2), the first chip having a first active surface, a first back surface opposite to the first active surface, a first wire-bonding pad (Fig. 2, 2a) and a first bump-bonding pad (Fig 3, 10 and Col 5 Ln 50), wherein the first wire-bonding pad and the first bump-bonding pad are formed on the first active surface;

a second chip disposed above the main substrate (Fig. 2, 3), the second chip having a second active surface, a second back surface opposite to the second active surface, a second wire-bonding pad (Fig. 2,

3a) and a second bump-bonding pad (Fig. 3, 10 and Col 5 Ln 50), wherein the second wire-bonding pad and the second bump-bonding pad are formed on the second active surface;

an interconnection substrate having a first chip-connecting contact, a second chip-connecting contact and a circuit connecting the first chip-connecting contact and the second chip-connecting contact (Fig. 2, 1),

a first bump interposed between the first chip connecting contact and the first bump-bonding pad (Fig. 3, 10);

a second bump interposed between the second chip connecting contact and the second bump-bonding pad (Fig. 3, 10);

a plurality of wires electrically connecting the first wire-bonding pad and the second wire-bonding pad to the contacts respectively (Fig. 2, 5).

With respect to **claim 2**, Misumi teaches a multi-chip module comprising an encapsulation covering the first ship, the second chip, and the upper surface of the main substrate (Fig. 2, 8)

With respect to **claim 3**, Misumi teaches that the interconnection substrate is a die-substrate (Fig. 2, 1 and Col 4 Ln 14).

With respect to **claim 4**, Misumi teaches that the main substrate is a lead frame (Fig. 2, 4 and 17).

With respect to **claim 13**, Misumi teaches a plurality of solder balls attached to ball pads of the lower surface of the main substrate (Fig. 2, 7).

With respect to **claim 18**, Mitsumi teaches a multi-chips module package comprising:

a main substrate having an upper surface and a plurality of contacts (Fig. 2, 4),

a first chip disposed above the main substrate (Fig. 2, 2), the first chip having a first active surface, a first back surface opposite to the first active surface, a first wire-bonding pad (Fig. 2, 2a) and a first bump-bonding pad (Fig 3, 10 and Col 5 Ln 50), wherein the first wire-bonding pad and the first bump-bonding pad are formed on the first active surface;

a second chip disposed above the main substrate (Fig. 2, 3), the second chip having a second active surface, a second back surface opposite to the second active surface, a second wire-bonding pad (Fig. 2, 3a) and a second bump-bonding pad (Fig. 3, 10 and Col 5 Ln 50), wherein the second wire-bonding pad and the second bump-bonding pad are formed on the second active surface;

an interconnection substrate having a first chip-connecting contact, a second chip-connecting contact and a circuit connecting the first chip-connecting contact and the second chip-connecting contact (Fig. 2, 1), the interconnection substrate attached to the first chip and the second chip directly through solder materials (Fig. 2, 10);

a plurality of wires connecting the first wire-bonding pad and the second wire-bonding pad to the contacts respectively (Fig. 2, 5).

With respect to **claim 19**, Misumi teaches a multi-chip module comprising an encapsulation covering the first chip, the second chip, and the upper surface of the main substrate (Fig. 2, 8).

With respect to **claim 20**, Misumi teaches that the interconnection substrate is a die substrate (Fig. 2, 1 and Col 4 Ln 14).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Misumi, in view of Hung et al (U.S. Patent #6476469), hereafter known as Hung.

With respect to **claim 4**, Misumi teaches all of the limitations of claim 1, but does not teach that the main substrate is a lead frame. Hung teaches a main substrate that is a lead frame (Fig. 3d, 202 and Col 3 Ln 52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Misumi and Hung to se a lead frame for the main substrate in order to facilitate a connection to other packages.

With respect to **claim 5**, Misumi teaches all of the limitations of claim 1, but does not teach a main substrate that is a quad flat non-leaded lead-frame. Hung teaches a main substrate that is a quad flat non-leaded lead-frame (Fig. 3d). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Misumi and Hung to use a quad flat non-leaded lead-frame as a main substrate in order to reduce signal attenuation in the package (Col 3 Ln 48).

Claims 6-8, 10, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Misumi, in view of Farnworth et al (U.S. Patent #6097087), hereafter known as Farnworth.

With respect to **claim 6**, Misumi teaches all of the limitations of claim 1, but does not teach that the first bump is a metal bump. Farnworth teaches metal bumps (Col 2 Ln 25). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Misumi and Farnworth to use metal bumps in order to improve the structural and electrical connection.

With respect to **claim 7**, Misumi teaches all of the limitations of claim 1, but does not teach an electrically conductive plastic bump. Farnworth teaches electrically conductive plastic bumps (Col 7 Ln 32). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine

the teachings of Misumi and Farnworth to use conductive plastic bumps in order to enhance the structural integrity of the package.

With respect to **claim 8**, Misumi teaches all of the limitations of claim 1, but does not teach that the material of the second bump comprises epoxy. Farnworth teaches a bump with material comprising epoxy (Col 5 Ln 22). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Misumi and Farnworth to use a material comprising epoxy in order to enhance the structural integrity of the package.

With respect to **claim 10**, Farnworth teaches a gold bump (Col 2 Ln 63).

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Misumi and Farnworth, further in view of Fukuoka (U.S. Patent #6949654).

With respect to **claim 11**, Misumi and Farnworth teach all of the limitations of claim 6, but do not teach a lead-free bump. Fukuoka teaches a lead-free bump (Fig. 1, 107). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Misumi, Farnworth, and Fukuoka to use a lead-free bump in order to avoid the health and environmental concerns related to lead.

Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Misumi, in view of Neuhaus et al (U.S. PG Pub #2002/0027294), hereafter known as Neuhaus.

With respect to **claim 14**, Misumi teaches all of the limitations of claim 1 but does not teach a passive component disposed on the interconnection substrate. Neuhaus teaches a passive component disposed on a substrate (Fig. 1, 110 and Paragraph 0049). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Misumi and Neuhaus to dispose a passive component on the substrate in order to increase the electrical capabilities of the substrate.

With respect to **claim 15**, Neuhaus teaches that the passive component is a capacitor (P 0049).

Claims 9 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Misumi, in view of Felten (U.S. Patent #6317023).

With respect to **claim 9**, Misumi teaches all of the limitations of claim 1, but does not teach that the interconnection substrate is an organic substrate. Felten teaches a substrate that is an organic substrate (abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Misumi and Felten to make an organic interconnection substrate in order to make the device compliant for use in commercial applications which require an organic substrate.

With respect to **claim 16**, Misumi teaches all of the limitations of claim 1, but does not teach a passive component embedded in the interconnection substrate. Felten teaches a passive component embedded in a substrate (abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Misumi and Felten to embed a passive component in the interconnection substrate in order to decrease the size of the package.

Claims 17 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Misumi, in view of Hsuan et al (U.S. Patent #6239367), hereafter known as Hsuan.

With respect to **claim 17**, Misumi teaches all of the limitations of claim 2, but does not teach that the interconnection substrate is exposed out of the encapsulation. Hsuan teaches a substrate that is exposed out of an encapsulation (Fig. 3, 82 and 76). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Misumi and Hsuan to expose the interconnection substrate out of the encapsulation in order to decrease the overall size of the package and to provide a heat dissipation path.

With respect to **claim 21**, Misumi teaches all of the limitations of claim 20, but does not teach that the interconnection substrate is exposed out of the encapsulation. Hsuan teaches a substrate that is exposed out of an encapsulation (Fig. 3, 82 and 76). It would have been obvious to one of ordinary

skill in the art at the time the invention was made to combine the teachings of Misumi and Hsuan to expose the interconnection substrate out of the encapsulation in order to decrease the overall size of the package and to provide a heat dissipation path.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Misumi, in view of Ball (U.S. Patent #6407456).

With respect to **claim 12**, Misumi teaches all of the limitations of claim 1, but does not teach the main substrate comprising two chip pads for carrying the first and second chip. Ball teaches a substrate comprising two chip pads for carrying the first and second chip (Fig. 4, 20A and 20B). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Misumi and Ball to use two chip pads for carrying the first and second chip in order to mechanically and electrically secure the chips to the substrate.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ben P. Sandvik whose telephone number is (571) 272-8446. The examiner can normally be reached on Everyday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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